2A, Asynchronous Step-Down Regulator

Halogen Free

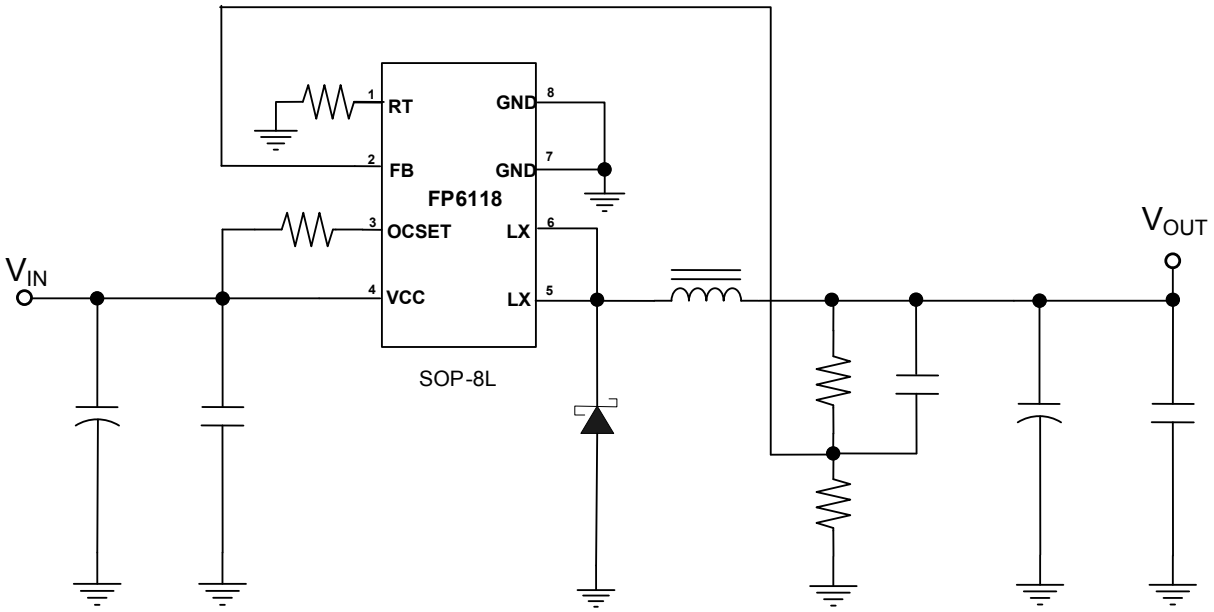
General Description

The FP6118 is a buck switching regulator for wide operating voltage application fields. The FP6118 includes a high current P-MOSFET, a high precision reference (0.8V) for comparing output voltage with a feedback amplifier, and an internal soft start timer and dead-time controller. The oscillator is for controlling the maximum duty cycle and PWM frequency.

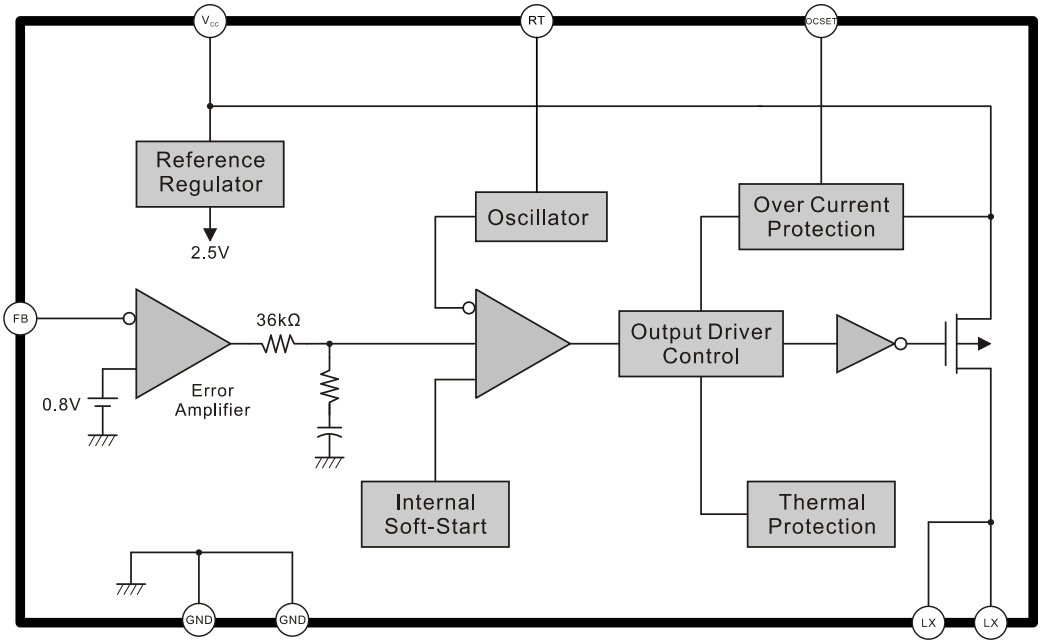
Features

- Precision Feedback Reference Voltage: 0.8V (2%)
- Wide Supply Voltage Operating Range: 3.6 to 30V
- Low Current Consumption: 3mA
- External Set Oscillator Frequency: 100 ~ 300KHz.
- Internal Soft-Start Function (SS)
- Built-In P-MOSFET for 2A Output Loading
- Over Current Protection
- Package: SOP-8L(EP)

Typical Application Circuit



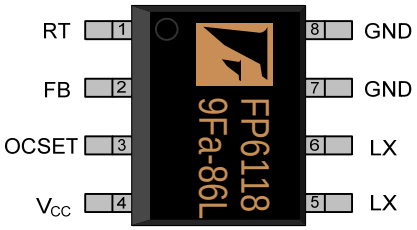
Function Block Diagram



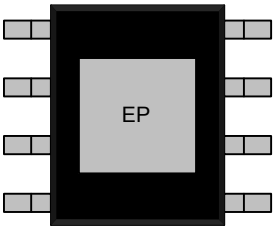
Pin Descriptions

SOP-8L(EP)

TOP View

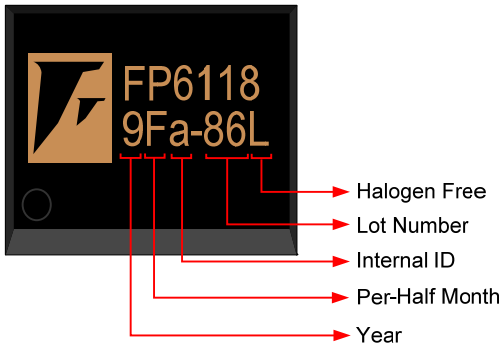


Bottom View



Name	No.	I / O	Description
RT	1	I	Connect a Resistor for Oscillator
FB	2	I	Error Amplifier Inverting Input
OCSET	3	I	Set Switch Output Over Current
V_{CC}	4	P	IC Power Supply (PMOS Source)
LX	5	O	PMOS High Current Output
LX	6	O	PMOS High Current Output
GND	7	P	IC Ground
GND	8	P	IC Ground
EP	9	P	Exposed PAD - Must connect to LX

Marking Information



Halogen Free: Halogen free product indicator

Lot Number: Wafer lot number's last two digits

For Example: 132386TB → 86

Internal ID: Internal Identification Code

Per-Half Month: Production period indicated in half month time unit

For Example: January → A (Front Half Month), B (Last Half Month)

February → C (Front Half Month), D (Last Half Month)

Year: Production year's last digit

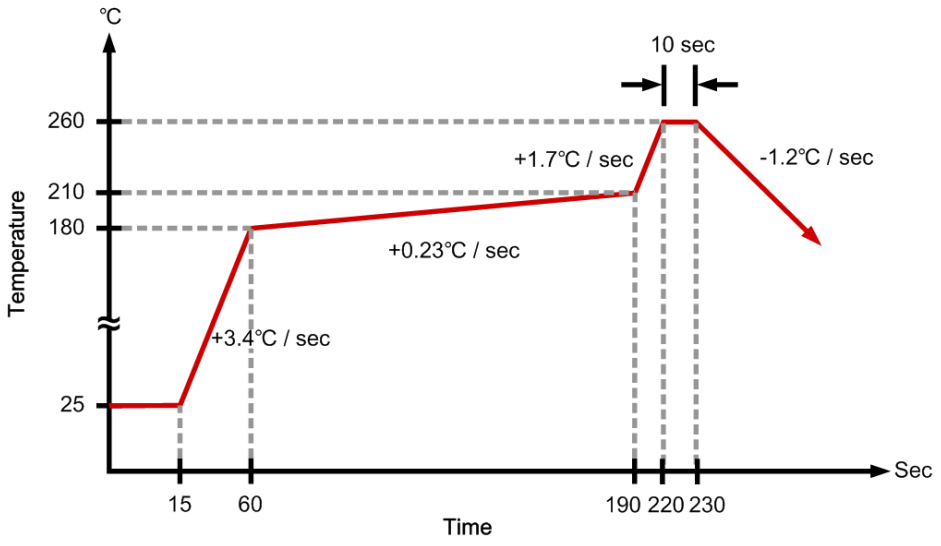
Ordering Information

Part Number	Operating Temperature	Package	MOQ	Description
FP6118XR-G1	-25°C ~ +85°C	SOP-8L(EP)	2500 EA	Tape & Reel

Absolute Maximum Ratings

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Power Supply Voltage	V_{CC}				30	V
Output Source Current					3.5	A
Error Amplifier Inverting Input			-0.3		1.2	V
Allowable Power Dissipation	P_D	SOP-8L(EP) $T_A \leqq +25°C$			1500	mW
Thermal Resistance Junction to Ambient	θ_{JA}	SOP-8L(EP)		+83		°C / W
Operating Temperature			-25		+85	°C
ESD Susceptibility		HBM (Human Body Mode)			2	KV
		MM (Machine Mode)			200	V
Storage Temperature	T_S		-55		+125	°C
Junction Temperature	T_J				+150	°C
Lead Temperature		(soldering, 10 sec)			+260	°C

IR Re-flow Soldering Curve



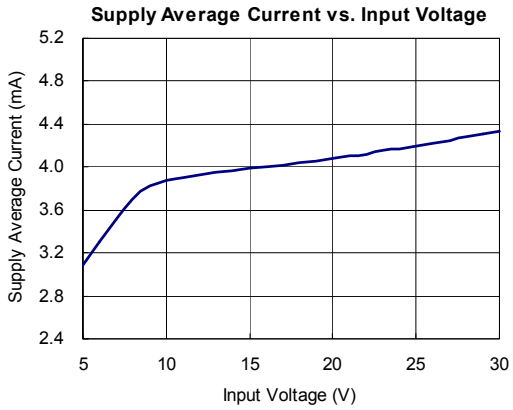
Recommended Operating Conditions

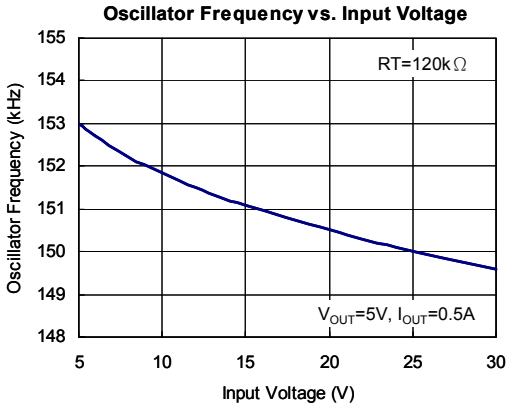
Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply Voltage	V_{CC}		3.6		30	V
Operating Temperature			-25		85	°C

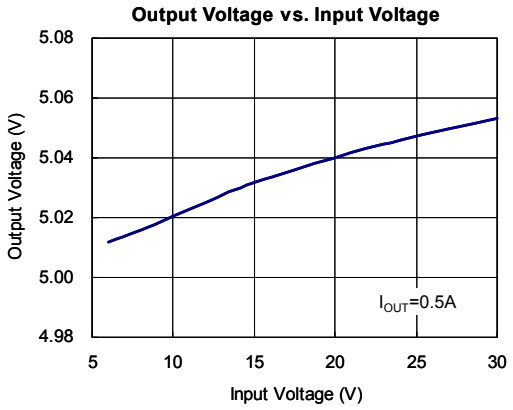
DC Electrical Characteristics (V_{CC}=6V, T_A = 25°C, unless otherwise noted)

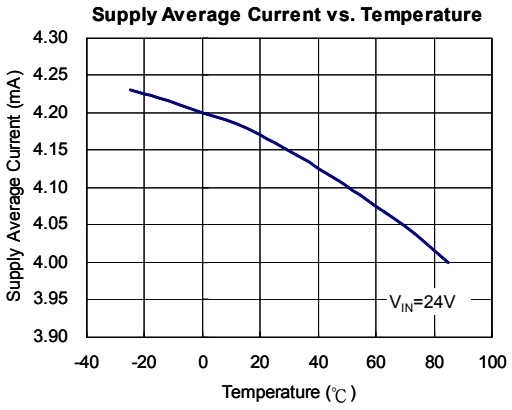
Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Reference						
Feedback Voltage	V_{REF}		0.784	0.8	0.816	V
Input Regulation	$\triangle V_{REF} / V_{REF}$	V_{CC}=3.6 V to 30 V		1	2	%
Feedback Voltage Change with Temperature	$\triangle V_{REF} / V_{REF}$	T_A=- -25°C to +85°C		1	2	%
Oscillator Section						
Oscillation Frequency	f	RT=120KΩ	135	150	165	KHz
Short Circuit or Over Current Oscillation Frequency	f_{SC}	Measured from LX pin waveform		40		KHz
Frequency Change with Voltage	Δf / ΔV	V_{CC}=3.6V to 30V		5		%
Frequency Change with Temperature	Δf / ΔT	T_A = -25°C to +85°C		5		%
Idle Period Adjustment Section						
Maximum Duty Cycle	T_{DUTY}	V_{FB} =0.2V		85		%
Output Section						
PMOS Switch Current	I_{LX}		-2			A
PMOS On Resistance	$R_{DS\ (ON)}$	V_{CC}=4.5V		70	95	mΩ
		V_{CC}=10V		50	60	mΩ
Thermal Shutdown Section						
Thermal Shutdown Temperature				+150		°C
Over Current Protection Section						
OCSET Bias Current	I_{OCSET}			40		μA
Total Device Section						
Supply Average current	I_{AVE}			4	6	mA

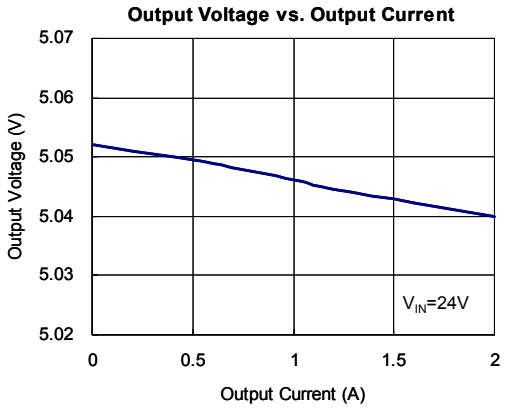
Typical Operating Characteristics

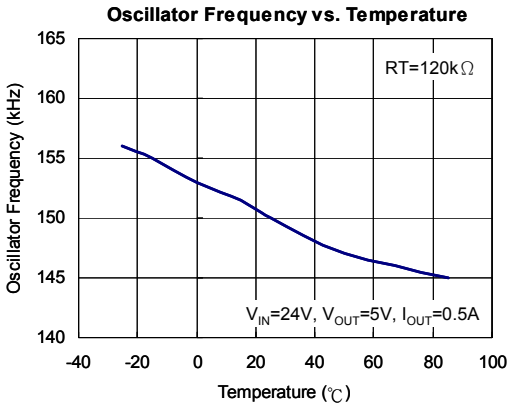




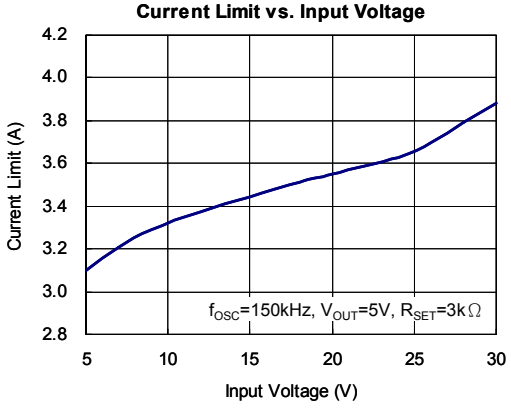




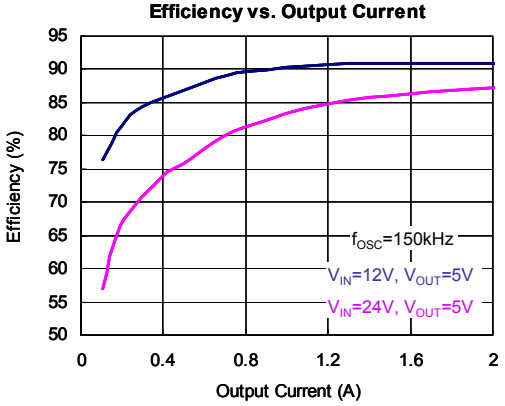




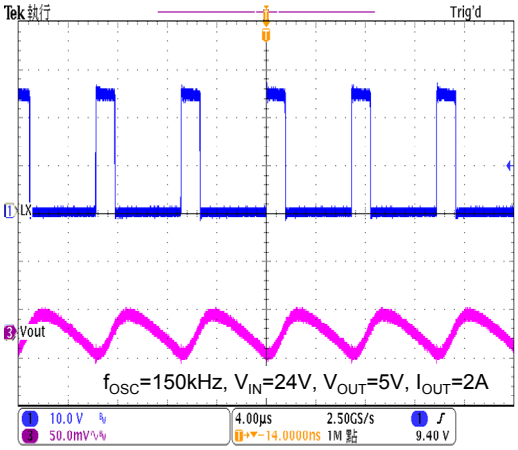
Current Limit vs. Input Voltage



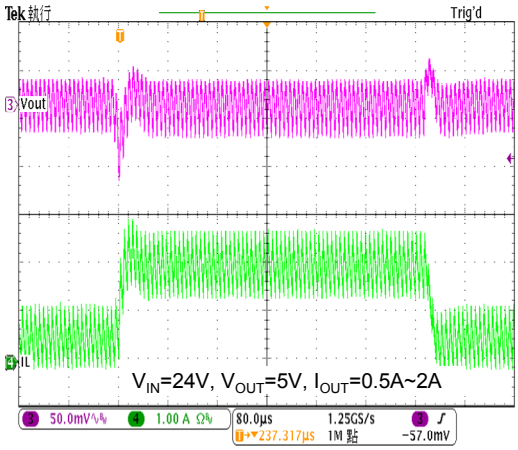
Efficiency vs. Output Current



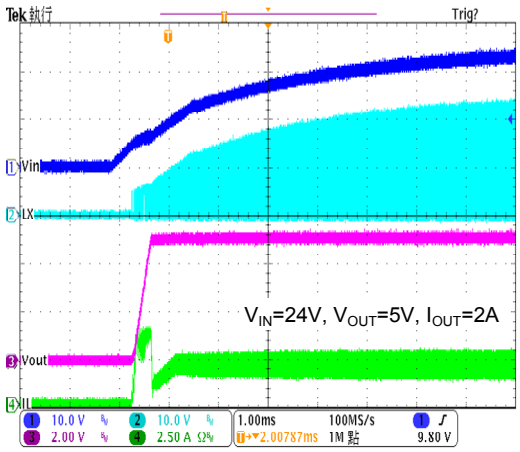
Output Ripple



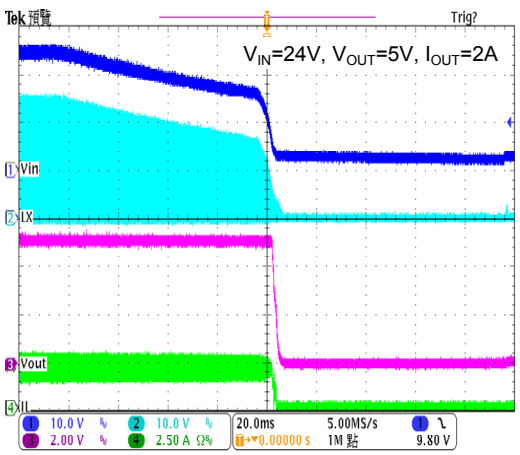
Load Transient Response



Power On



Power Off



Function Description

Voltage Reference

A 2.5V reference regulator supplies FP6118 internal circuits and uses a resistive divider to provide 0.8V precision reference voltage to the non-inverting terminal of error amplifier.

Error Amplifier

The error amplifier compares a sample of the DC-DC converter output voltage to the 0.8V (V_{REF}) reference and generates an error signal for the PWM comparator. Output voltage of the DC-DC converter is setting by the resistor divider with following equation (see Figure. 1)

$$V_{OUT} = 1 + \frac{R_3}{R_4} \times V_{REF}$$

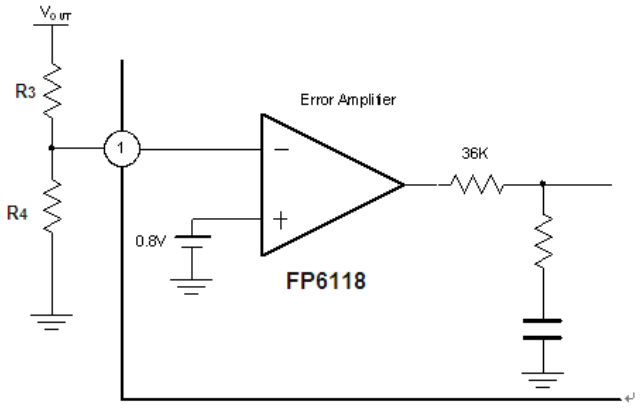


Figure 1. Error Amplifier with Feedback Resistance Divider

The recommended resistor value is summarized below:

V_{OUT} (V)	R_3 (kΩ)	R_4 (kΩ)
1.8	3k	2.4k
2.5	6.8k	3.2k
3.3	4.7k	1.5k
5	10.5k	2k

Oscillator

The oscillator frequency(f_{OSC}) can be set from 100KHz to 300KHz by connecting a resistor between RT and GND. Acceptable resistor values range from 220kΩ to 45kΩ. The oscillator frequency can be determined by using the table shown below:

RT(kΩ)	220	160	120	94	80	67	58	51	45
f_{osc}(KHz)	100	125	150	175	200	225	250	275	300

Thermal Protection

When a heavy loading draws current from the regulator, the chip temperature will rise. Once the junction temperature exceeds 150℃, FP6118 thermal protection function will be triggered and the LX output will be turned off. When junction temperature is lower, FP6118 starts again and enable LX pin output.

Over Current Protection

The FP6118 uses cycle-by-cycle current limit to protect the internal power switch. During each switching cycle, a current limit comparator detects if the power switch current exceeds the external setting current or not. Once over current occurs, chip will decrease the oscillator frequency to prevent from overheated. The current limit threshold is setting by external resistor (R_1) which is connecting from V_{CC} to OCSET pin. An internal 40μA current sink which draws current from the resistor sets the voltage at pin OCSET. Please refer to the following equation for setting the current limit value:

$$I_{OCP} = \frac{I_{OCSET} \times R_1}{35m\Omega}$$

Here, 35mΩ is the internal current sense resistance.

Example：

$$I_{OCP} = \frac{40\mu A \times 3k}{35m\Omega} = 3.43A$$

Application Information

Input Capacitor Selection

The input capacitor must be connected to the V_{CC} pin and GND pin of the FP6118 to maintain steady input voltage and filter out the pulsing input current. The voltage rating of input capacitor must be greater than maximum input voltage plus ripple voltage.

In switch mode, the input current is discontinuous in a buck converter. The source current waveform of the high-side MOSFET is a square wave. To prevent large voltage ripple, a low ESR input capacitor sized for the maximum RMS current must be used. The RMS value of input capacitor current can be calculated by:

$$I_{RMS} = I_{O\ MAX} \sqrt{\frac{V_O}{V_{IN}} 1 \quad \frac{V_O}{V_{IN}}}$$

It can be seen that when V_O is half of V_{IN}, C_{IN} is under the worst current stress. The worst current stress on C_{IN} is I_{O_MAX} / 2.

Inductor Selection

The value of the inductor is selected based on the desired ripple current. Large inductance gives low inductor ripple current and small inductance results in high ripple current. However, the larger value inductor usually has a larger physical size, higher series resistance, and lower saturation current. By experience, the value is to allow the peak-to-peak ripple current in the inductor to be 10%~20% maximum load current. The inductance value can be calculated by:

$$L = \frac{(V_{IN} - V_O)}{f \times \Delta I_L} \frac{V_O}{V_{IN}} = \frac{(V_{IN} - V_O)}{f \times [2 \times (10\% \sim 20\%) I_O]} \frac{V_O}{V_{IN}}$$

The inductor ripple current can be calculated by:

$$\Delta I_L = \frac{V_O}{f \times L} \times \left(1 - \frac{V_O}{V_{IN}}\right)$$

Choose an inductor that does not saturate under the worst-case load conditions, which is the load current plus half the peak-to-peak inductor ripple current, even at the highest operating temperature. The peak inductor current is:

$$I_{L\_PEAK} = I_O + \frac{\Delta I_L}{2}$$

The inductors in different shape and style are available from manufacturers. Shielded inductors are small and radiate less EMI issue. But they cost more than unshielded inductors. The choice depends on EMI requirement, price and size.

Inductor Value (μH)	Dimensions(mm)	Component Supplier	Model
10	10.3×10.3×4.0	FENG-JUI	TPRH10D40-10R
10	10.1×10.1×3.0	Sumida	CDRH104R
15	10.3×10.3×4.0	FENG-JUI	TPRH10D40-15R

Output Capacitor Selection

The output capacitor is required to maintain the DC output voltage. Low ESR capacitors are preferred to keep the output voltage ripple low. In a buck converter circuit, output ripple voltage is determined by inductor value, switching frequency, output capacitor value and ESR. The output ripple is determined by:

$$\Delta V_O = \Delta I_L \times \left(ESR_{C_{OUT}} + \frac{1}{8 \times f \times C_{OUT}} \right)$$

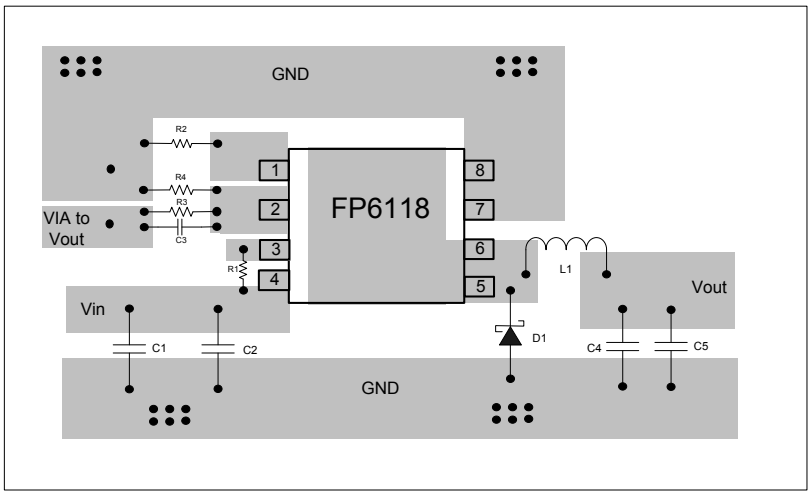
Where f = operating frequency, C_{OUT}= output capacitance and ΔI_L = ripple current in the inductor. For a fixed output voltage, the output ripple is highest at maximum input voltage since ΔI_L increases with input voltage.

Using Ceramic Input and Output Capacitors

Care must be taken when ceramic capacitors are used at the input and the output. When a ceramic capacitor is used at the input and the power is supplied by a wall adapter through long wires, a load step at the output can induce ringing at the input, V_{IN}. In best condition, this ringing can couple to the output and be mistaken as loop instability. In worst condition, a sudden inrush of current through the long wires can potentially generate a voltage spike at V_{IN}, which may large enough to damage the part. When choosing the input and output ceramic capacitors, choose the one with X5R or X7R dielectric formulations. These dielectrics have the best temperature and voltage characteristics of all the ceramics for a given value and size.

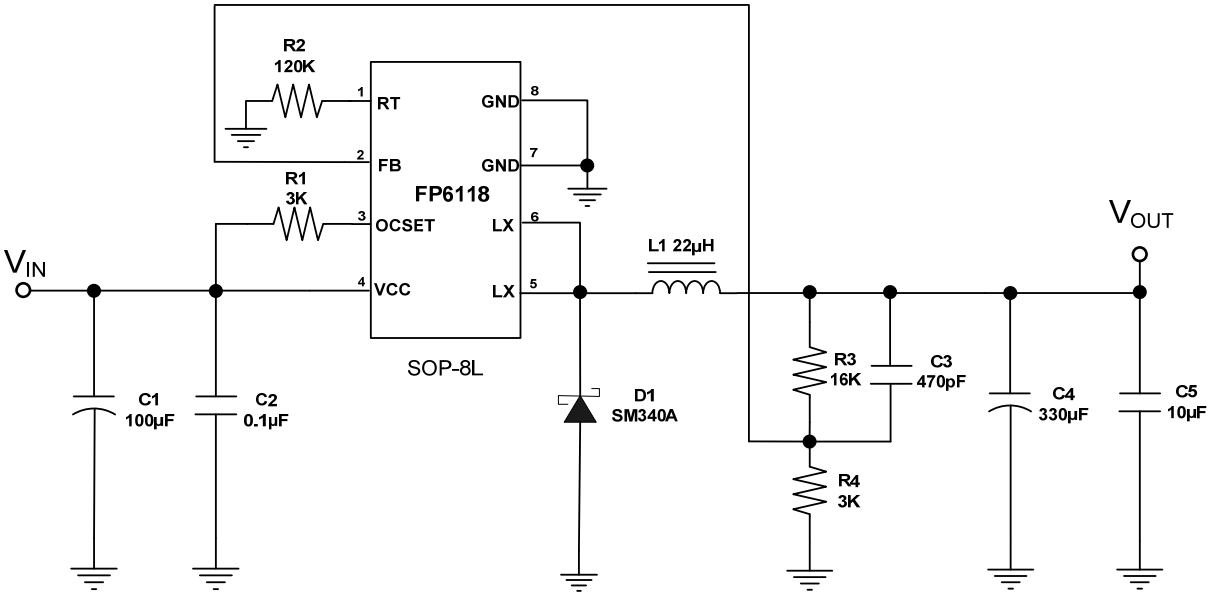
PC Board Layout Checklist

1. The power traces, consisting of the GND trace, the LX trace and the V_{IN} trace should be kept short, direct and wide.
2. Place C_{IN} near V_{CC} pin as closely as possible to maintain input voltage steady and filter out the pulsing input current.
3. The resistive divider R_3 and R_4 must be connected to FB pin directly as closely as possible.
4. FB is a sensitive node. Please keep it away from switching node, LX. A good approach is to route the feedback trace on another layer and to have a ground plane between the top layer and the layer on which the feedback trace is routed. This reduces EMI radiation on to the DC-DC converter's own voltage feedback trace.
5. Keep the GND plates of C_{IN} and C_{OUT} as close as possible. Then connect this to the ground plane (if one is used) with several vias. This reduces ground plane noise by preventing the switching currents from circulating through the ground plane. It also reduces ground bounce at the FP6118 GND pin by giving it a low impedance ground connection.



FP6118 Suggested Layout

6. Typical Application:



FP6118 Basic DC-DC Regulator Circuits

For example:

The V_{IN} power supply is 12V and the V_{OUT} is designed for 5.0V / 2A solution.

The output voltage equation is:

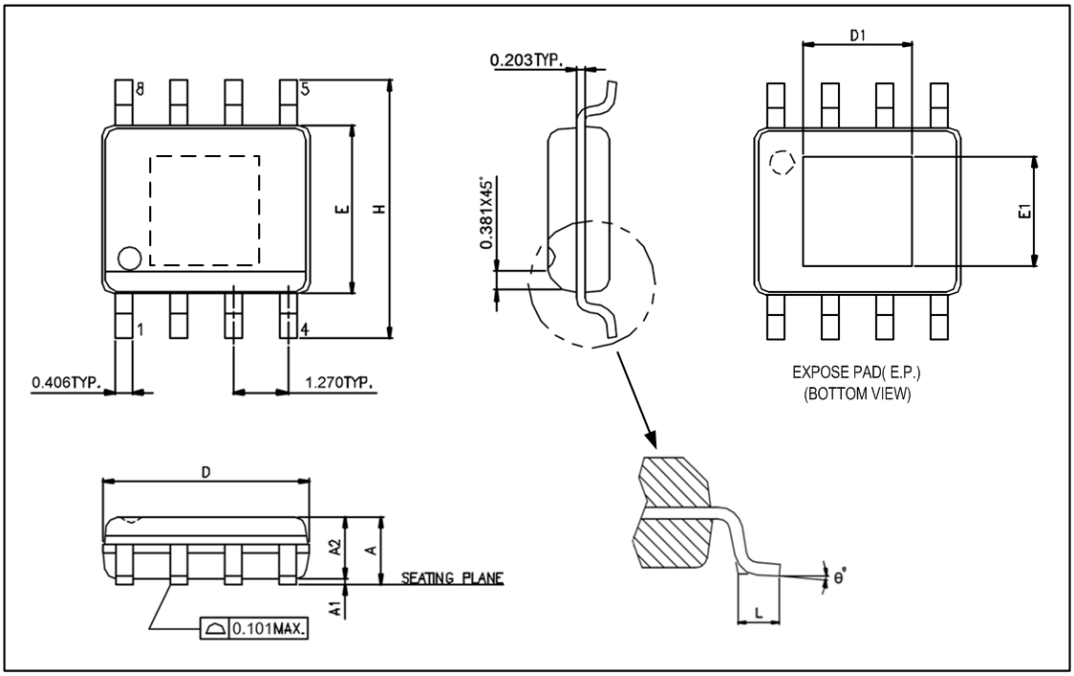
$$V_{OUT} = 1 + \frac{R_3}{R_4} \times V_{REF} = 1 + \frac{10.5K\Omega}{2K\Omega} \times 0.8V = 5.0V$$

Recommended Parameter Selection

V_{OUT} (V)	f_{OSC}(KHz)	R3 (kΩ)	R4 (kΩ)	L (μH)	C3(pF)	C_1 (μF)	C_4 (μF)
1.8	150	3	2.4	15	270~470	100	330
2.5	150	6.8	3.2	15	270~470	100	330
3.3	150	4.7	1.5	22	270~470	100	330
5	150	10.5	2	22	270~470	100	330

Package Outline

SOP-8L (EP)



Unit: mm

Symbols	Min. (mm)	Max. (mm)
A	1.346	1.752
A1	0.050	0.152
A2		1.498
D	4.800	4.978
E	3.810	3.987
H	5.791	6.197
L	0.406	1.270
θ°	0°	8°

Exposed PAD Dimensions:

Symbols	Min. (mm)	Max. (mm)
E1	2.184 REF	
D1	2.971 REF	

Note:

1. Package dimensions are in compliance with JEDEC outline: MS-012 AA.
2. Dimension ”D” does not include molding flash, protrusions or gate burrs.
3. Dimension “E” does not include inter-lead flash or protrusions.